Meridian 1

Clock Controller Description and Installation

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This document is issued to include new material provided from verification and validation of product.

Contents

Clock Controller Description and Installation

Contents

The following are the topics in this section:

Reference list

The following are the references in this section:

- *Option 11C 1.5Mb DTI/PRI* (553-3011-310)
- *Option 11C 2.0Mb DTI/PRI* (553-3011-315)

Introduction

This chapter introduces the NTRB53 Clock Controller, and provides procedures on how to install this clock controller on Meridian 1 Options 51C, 61C, and 81C.

The NTRB53 Clock Controller replaceS the QPC471H and QPC775F in new systems. QPC471H and QPC775F Clock Controllers will continue to be supported.

Note 1: The description section of this chapter applies to all supported Meridian 1 systems, that is, Options 11C, 51C, 61C, and 81C. However, the installation procedures apply only to Options 51C, 61C, and 81C. For Option 11C specific information, refer to *Option 11C 1.5Mb DTI/PRI* (553-3011-310) and *Option 11C 2.0Mb DTI/PRI* (553-3011-315).

Also, the illustrations used in the description section depict an Option 11C. However, the system may also be representative of an Option 51C, 61C, or 81C.

Description

This section summarizes the use of clock controllers on Meridian 1 Option 11C, 51C, 61C, and 81C. For Meridian 1 large systems, the following clock controllers are supported:

- NTRB53 - available for all markets
- QPC471 - available for U.S. markets. Vintages A through G of the QPC471 Clock Controller can be used in one system; vintage H of QPC471 Clock Controllers cannot be mixed with clock controllers of other vintages.
- QPC775 - available for only the Canadian and International markets

Note: Clock controllers cannot be mixed in one system.

Need for synchronization

Digital trunking requires synchronized clocking so a shift in one clock source results in an equivalent shift of the same size and direction in all parts of the network.

When digital signals travel over a communication link, the receiving end must operate at the same frequency (data rate) as the originating end to prevent loss of information. This is referred to as link synchronization. If both ends of a communication link are not in synchronization, data bit slips occur resulting in a loss of data. In general, accurate timing is very important, but synchronized timing is a must for reliable data transfer.

When only two Meridian 1 switches are interconnected, synchronization can be achieved by operating the two systems in a master/slave mode whereby one system derives timing from the other. However, in a network of digital systems, slips can be better prevented by forcing all digital systems to use a common reference clock (see Figure 1 on page 13).

Supported Clock Controllers

For Meridian 1 large systems, the following clock controllers are supported:

- NTRB53
- QPC471
- QPC775

NTRB53 Clock Controller

Introduced with Release 25.40, the NTRB53 Clock Controller is a replacement for the QPC471 and QPC775 Clock Controllers. The NTRB53 clock controller retains existing functionality.

Software configuration of the clock remains unchanged. Release 25.40 software introduces a Peripheral Software Download (PSDL) object to allow field upgrades of the clock's firmware. Overlay changes allow for force download and status checking. Support for the IDC command and hardware inventory are also included.

See Table 1 for NTRB53 Clock Controller compatiblity with systems and software releases.

Table 1
NTRB53 card compatibility guide

Meridian 1	Release 25.40	Release 19 to 25.3x
Option 11C/Mini	No	No
Option 21E	No	Yes
Option 51	No	Yes
Option 51C	Yes	Yes
Option 61	No	Yes
Option 61C	Yes	Yes
Option 71	No	Yes
Option 81	No	Yes
Option 81C	Yes	Yes

Note: PSDL enhancements will not be available for software prior to Release 25.40.

System Initialization

During system initialization, system software verifies if clock controllers in the system are downloadable (NTRB53). If the clock controllers are downloadable, then both downloadable clock controller cards will be checked for their current software version number. This version number is compared with the version number of the PSDL file stored in the Meridian 1 software database.

If there is a mismatch between the two version numbers and the Meridian 1 database has the higher version number, the card will be put in the PSDL downloading tree. Once the entry is added in the PSDL tree, the preprocess step is done. The next step is for the system to initiate the downloading in the background, using the PSDL tree. As soon as the download complete message is received from the card, the CPU sends a message to reset the clock controller card so that it boots with the new software. Once a selftest is complete the core sends an enable base message to enable the card.

Maintenance Overlays

Downloading can be initiated from Overlay 60 for the inactive clock controller card as part of the enabling sequence of the card. A download can be forced by specifying the optional parameter FDL (Force Download) when enabling the card. At the prompt, enter:

ENL CC x FDL	Enable Clock in side x with the force download option

If the optional parameter is not specified, then downloading is conditional. This means that the version number of the loadware on the clock controller card will be checked against the version number on the Meridian 1 disk. If a mismatch is found and the version number in the Meridian 1 software database is higher, then downloading will be initiated for that card. The entry for the card is not added to the PSDL tree at this time. Instead, downloading is initiated on a single card and only that card will be allowed to perform the force download option.

QPC471 and QPC775 Clock Controllers

Clock Controllers QPC471 and QPC775 will continue to function with software Release 25.40 and above on the following systems:

- Meridian 1 Option 51C
- Meridian 1 Option 61C
- Meridian 1 Option 81C

Note: See “Description” on page 8. for market and application availability information.

Synchronization methods

There are two common methods of operation for maintaining timing coordination between switching systems: Plesiosynchronous and Mesosynchronous.

Plesiosynchronous operation

In a Plesiosynchronous operation, nodal clocks run independently (free run) at the same nominal frequency. There are frequency differences between clocks resulting in frame slips (see "Frame slip" on page 14.) The magnitude of frame slips are directly proportional to the frequency difference. Slips are inevitable but can be minimized by using very stable clocks and elastic stores or buffers. These buffers can absorb data bits to compensate for slight variances in clock frequencies.

Mesosynchronous operation

In a Mesosynchronous operation, nodal clocks are continuously and automatically locked to an external reference clock. With this method, frame slips can be eliminated if elastic stores are large enough to compensate for transmission variances. Thus, Mesosynchronous operation can be virtually slip free.

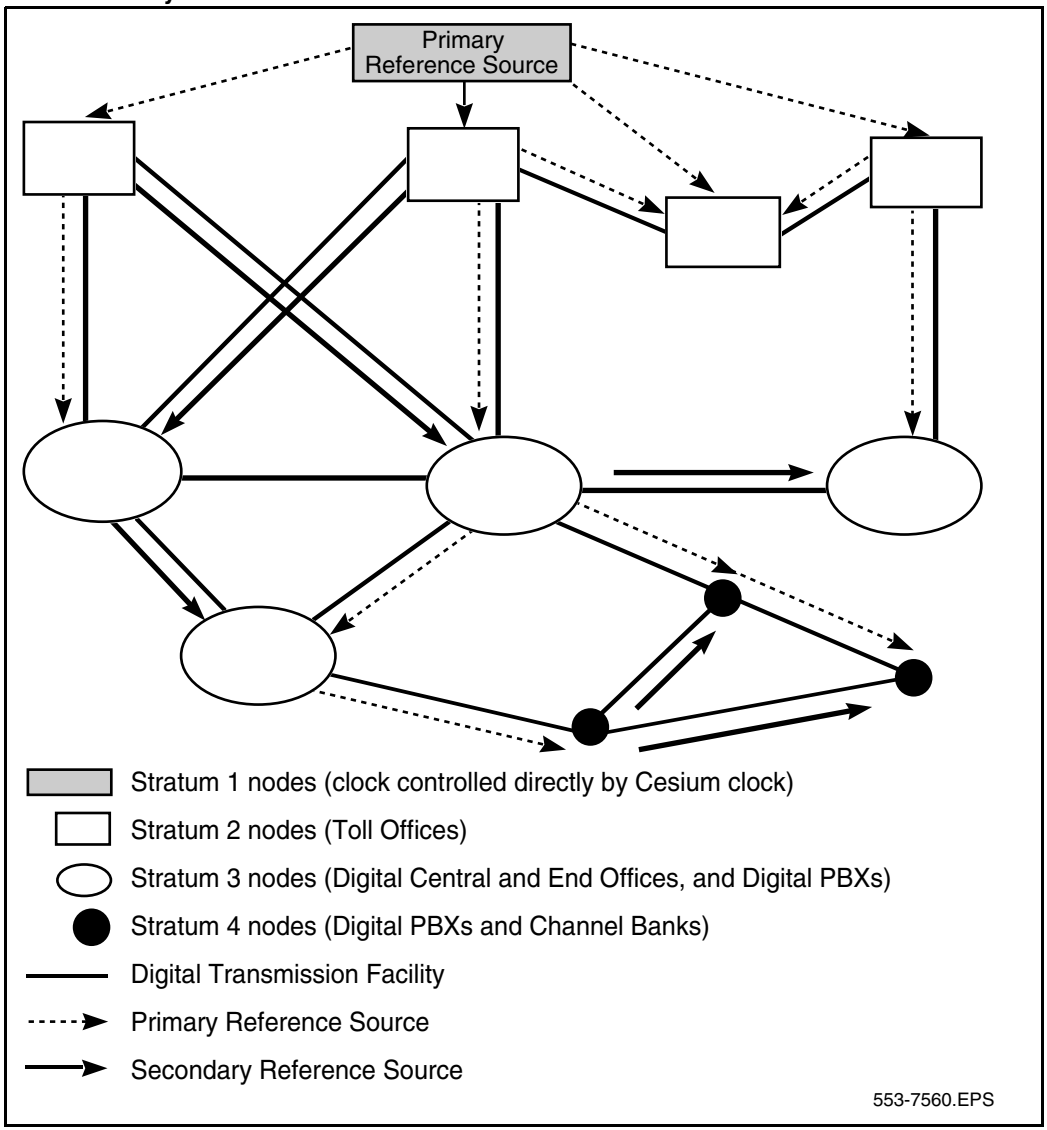
Whenever possible, the Meridian 1 switch operates in Mesosynchronous by using clock controller circuit cards to lock onto an external reference source, such as the Central Office, another Meridian 1 switch, and so on. This statement is true unless the Meridian 1 is used as a Master in an independent/private network with no digital links to a higher Node Category.

In an isolated private network, the Meridian 1 clock controller can operate in free run mode and act as a master clock to be tracked by other switch systems in the private network.

Hierarchical synchronization

Figure 1 on page 13 provides a general view of Digital Network Clock Synchronization including the four stratum level Node Categories. Stratum 1 being the most accurate and Stratum 4 being the least accurate. Meridian 1 clocking meets Node Category E Stratum 4 requirements. Also shown are ways of providing a Secondary Clock Source while preventing timing loops.

Figure 1
Hierarchical Synchronization



Stratum levels

In a digital network, nodes are synchronized using a priority master/slave method. Digital nodes are ranked in Stratum levels 1 to 5. Each node is synchronized to the highest ranking node in its neighborhood with which it has a direct link. Refer to Table 2.

Table 2
Node categories and stratum levels

	Stratum 2	**Stratum 3**	**Stratum 4**
Accuracy	+/- 1.6 * 10^{-8} Hz	+/- 4.6 * 10^{-6} Hz	+/- 3.2 * 10^{-5} Hz
Holdover	1 * 10^{-10} per day	<= 255 frame slips in 1st 24 hours	Not Required
Hardware Duplication	Required	Required (Note 1)	Not Required
MTIE During Rearrangement	MTIE <= 1 usec Phase Change Slope: <= 81 ns in any 1.326 msec	MTIE <= 1 usec Phase Change Slope: <= 81 ns in any 1.326 msec	No Requirement (Note 2)
Pull-in Range	3.2 * 10^{-8} Hz	9.2 * 10^{-6} Hz	6.4 * 10^{-5} Hz
Dedicated Timing Required	Required	Required	Not required

Note 1: Non-duplicated clock hardware that meets all other stratum 3 requirements is referred to as stratum 3ND.

Note 2: Stratum 4 clock hardware that meets MTIE requirements during rearrangements is referred to as 4E.

Frame slip

Digital signals must have accurate clock synchronization for data to be interleaved into or extracted from the appropriate timeslot during multiplexing and demultiplexing operations. A Frame Slip is defined (for 2 Mbyte links) as the repetition or deletion of the 256 data bits of a CEPT frame due to a sufficiently large discrepancy in the read and write rates of the buffer (clocks are not operating at exactly the same speed).

When data bits are written into (added to) a buffer at a slightly *higher* rate than they are read (emptied), sooner or later the buffer overflows. This is a slip-frame deletion.

In the opposite situation, when data bits are written (added) into a buffer at slightly *lower* rate than they are read (emptied), eventually the buffer runs dry or underflows. This is also a slip-frame repetition.

A 1.5 Mbyte PRI contains a buffer large enough to hold about 2 full DS-1 frames (193 x 2 = 386). A 2 Mbyte PRI contains a buffer large enough to contain 2 full frames (256 x 2 = 512 bits). The buffer is normally kept half full (1 frame).

Slippage impacts data transfer, as is shown in Table 3. Proper clock synchronization can control or avoid the degradations shown.

Table 3
Performance impact of one slip on service type

Service	Potential Impact
Encrypted Text	Encryption key must be resent.
Video	Freeze frame for several seconds. Loud pop on audio.
Digital Data	Deletion or repetition of data. Possible misframe.
Facsimile	Deletion of 4 to 8 scan lines. Dropped call.
Voice Band Data	Transmission Errors for 0.01 to 2 s. Dropped call.
Voice	Possible click.

Guidelines

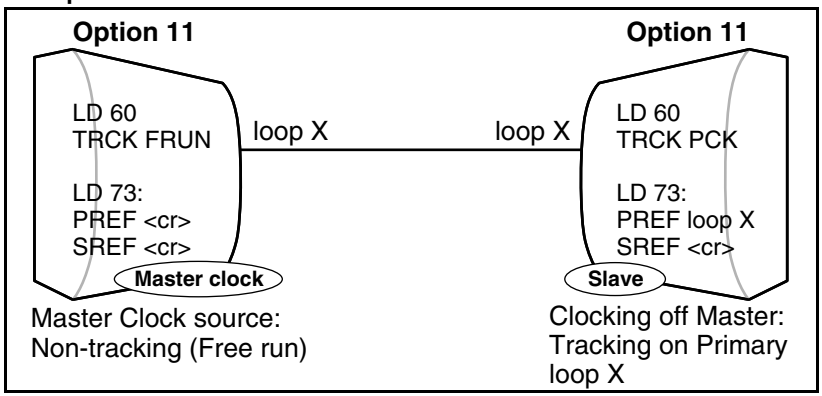
Listed below are a few key points about designing Network Synchronization:

- Where possible, the Master Clock Source should always be from a Node Category/Stratum with higher clock accuracy, that is, a PBX connected to the Central Office (CO.) The CO is the Master and the PBX is the Slave.
- The source should not be in free-run itself (providing its own clock) unless it operates in a fully independent network where the source acts as Master (see “Plesiosynchronous operation” on page 12.)

- When connecting two PBXs together (no CO connections), the most reliable PBX should be the Master. Reliability here refers to the clock controller's Dual CPU/Dual Clock, battery back-up or stratum level.
- Avoid timing loops. A timing loop occurs when a clock using as its reference frequency a signal that is itself traceable to the output of that clock. The formation of such a closed timing loop leads to frequency instability and is not permitted. Timing loops are sometimes unavoidable on the secondary clock reference source.
- Ensure all CO/PBX links used as clock references have a traceable path back to the same stratum 1 clock source.

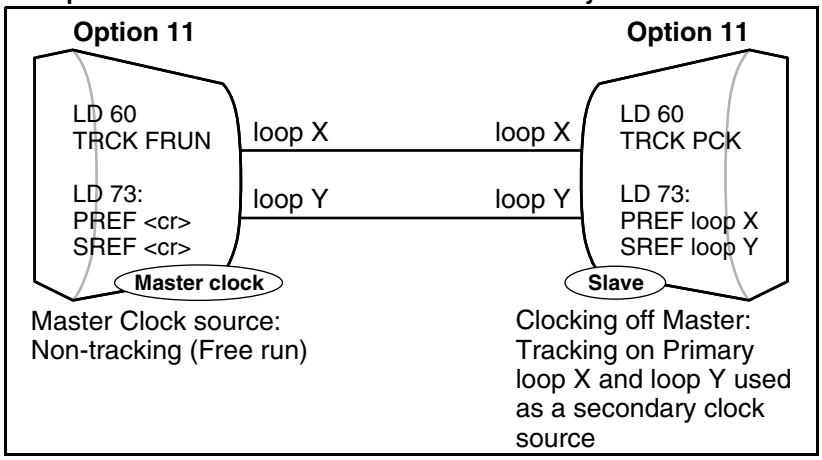
While it is beyond the scope of this discussion to provide detailed Network Synchronization, the examples in Figure 2 and Figure 3 illustrate some basic concepts to achieve stable clocking.

Figure 2
Example 1: Isolated Private Network



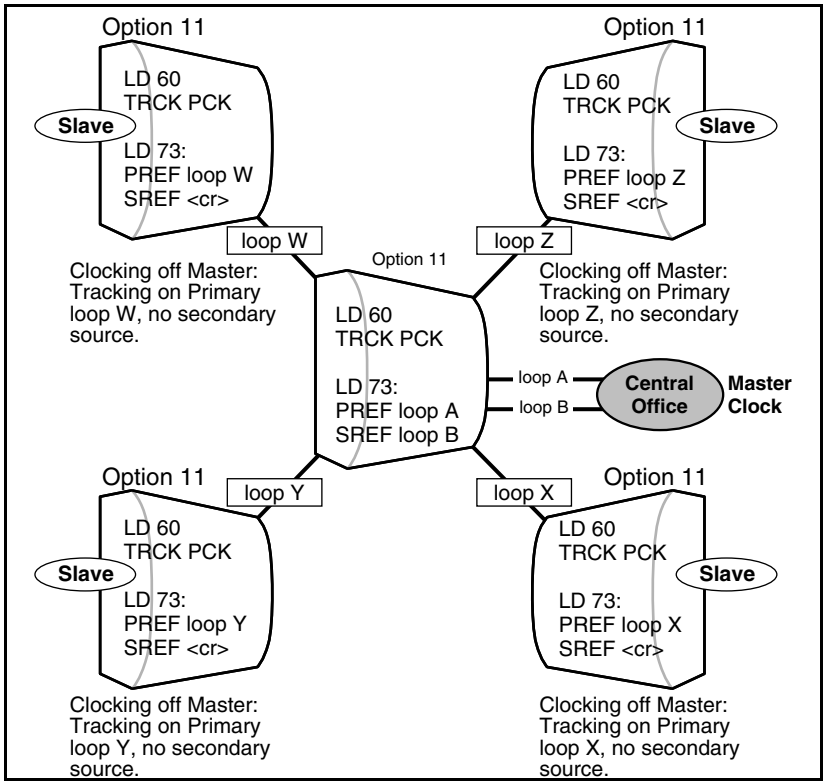
In Figure 2, there is no digital connection to the Central Office.

Figure 3
Example 2: Isolated Private Network with Secondary Reference Clock



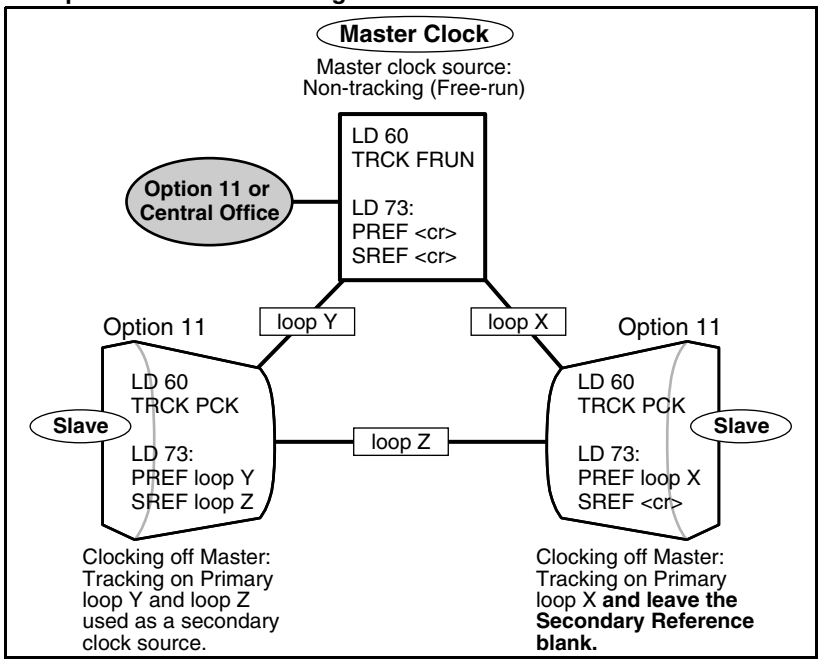
In Figure 3, there is no digital connection to the Central Office. For tie lines between PBXs facilitated by a central office, clocking is derived from the PBX, not the CO. When a second Digital loop is available, it can be used as a Secondary Clock source in case the Primary Source fails.

Figure 4
Example 3: Clocking Hierarchy referenced to a Public Network Master Clock



This is an example of a “STAR” arrangement— one Hub PBX links to the Central Office and all other PBXs connect as slaves. When a second Digital loop from the Meridian 1, which forms the hub of this network, becomes available, it can be used as a Secondary Clock Source if the Primary Source fails.

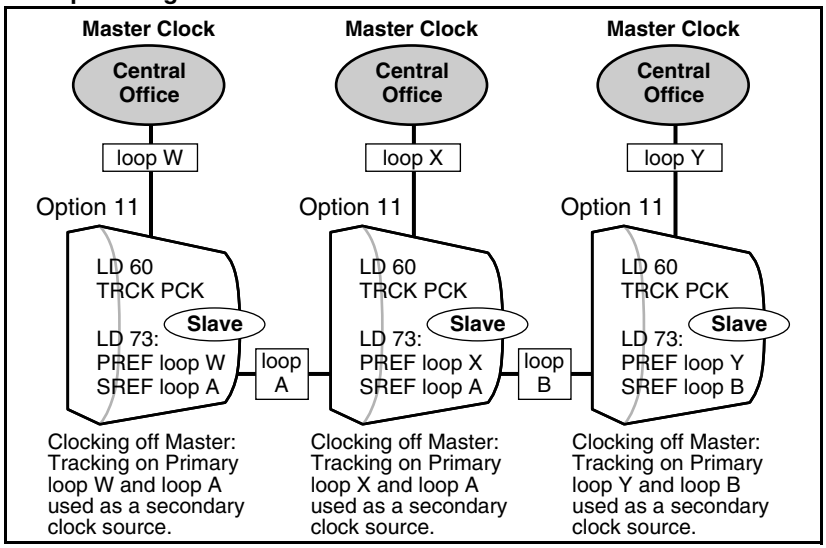
Figure 5
Example 4: Alternate Clocking from the same CO



In Figure 4, a digital connection to the Central Office may exist (that is, loops X and Y). When a second Digital loop from the CO or Master M-1 becomes available, it can be used as a Secondary Clock Source if the Primary Source fails.

To avoid timing loops, in example 4 the most reliable slave system should not have a Secondary Clock Source (SREF= <cr>). In this example, this is illustrated by the node that supports loops X and Z.

Figure 6
Example 5: Digital connection to the CO

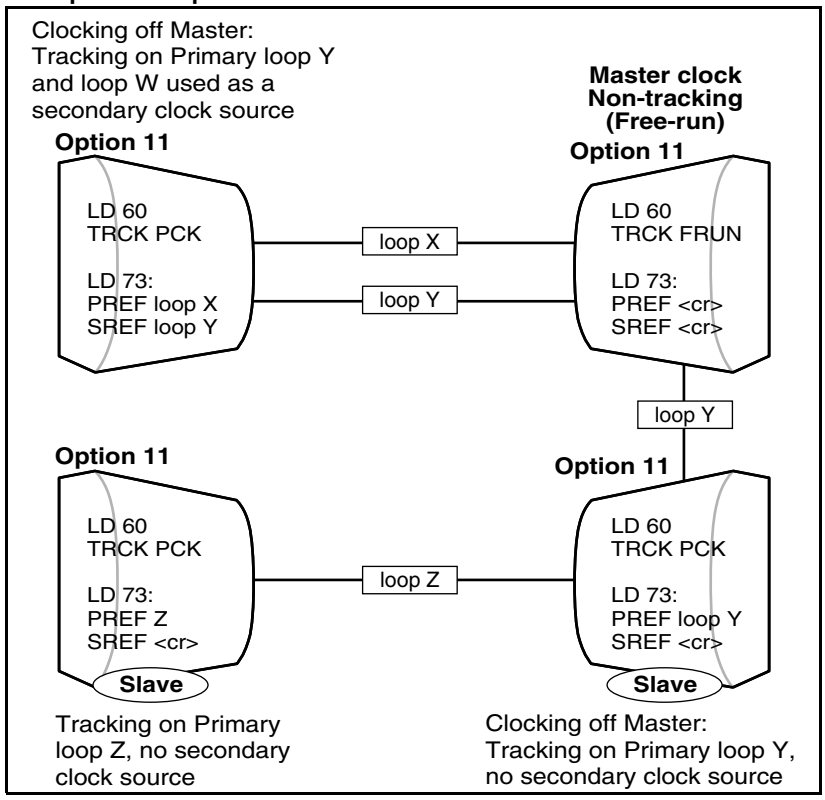


In Figure 6, digital connections to the Central Office exist. When a second digital loop from the CO becomes available, it can be used as a secondary clock source if the primary source fails.

Slaves can track each other as a secondary source since the chances are remote that both links to the Central Offices will go down at the same time.

All Central Offices must have a path back to the same Stratum 1 source.

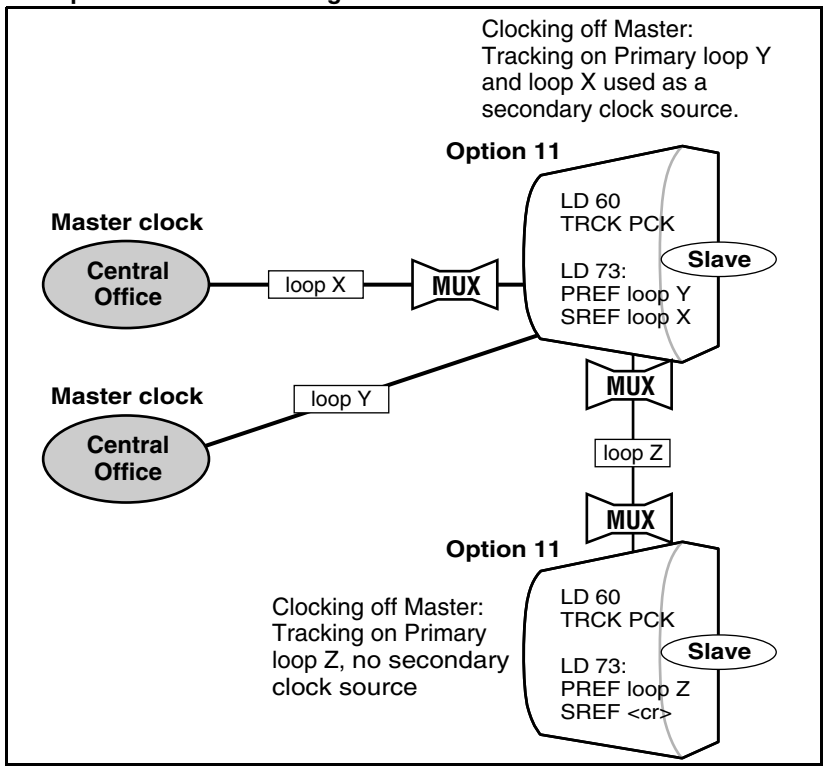
Figure 7
Example 6: Complex Isolated Private Network



Digital connections to the Central Office do not exist in Figure 7. If they do, the switch connected to the CO will track off the CO and in turn, be used as a clock source to other nodes.

When a second Digital loop from the Master Meridian 1/SL-1 becomes available, it can be used as a Secondary Clock Source if the Primary Source fails.

Figure 8
Example 7: Network Clocking with MUX



In Figure 8, the direct connection to the CO (without a MUX) should be used as a primary clock reference since there is the least amount of hardware involved. The MUX must pass the clock and not generate its own clock; in other words, it must also be a slave (not Free Run). Synchronized clocking is required.

Modes of operation

There are two modes of operation, tracking mode and free run (non-tracking) mode.

Tracking mode

In tracking mode, the Primary Rate Interface (PRI) or Digital Trunk Interface (DTI) loop supplies an external clock reference to the on-board clock controller. Two PRI or DTI packs can operate in tracking mode, with one defined as the primary reference source for clock synchronization, and the other defined as a secondary reference source. The secondary reference backs up the primary reference.

Free run (non-tracking) mode

The clock synchronization for a PRI loop can operate in free-run mode if:

- the loop is not defined as the primary or secondary clock reference
- the primary and secondary references are disabled
- the primary and secondary references are in a local alarm state

Option 11C Clock Controller daughterboard

The Option 11C supports a single on-board clock controller daughterboard, the NTAK20, located on one of the following cards:

- the NTRB21 1.5 Mbyte DTI/PRI card
- the NTAK09 1.5 DTI/PRI card
- the NTAK10 2 Mbyte DTI card
- the NTAK79 2 Mbyte PRI card
- the NTBK50 2 Mbyte PRI card

Clock controller circuitry synchronizes the Option 11C to an external reference clock and generates and distributes the clock to the system. This enables the Option 11C to function either as a external clock's slave or as a clocking master.

> ***Note:*** When configuring ISL over analogue trunks, clock controllers are not required.

Installation procedures

This section explains how to install a clock controller on Meridian 1 Options 51C, 61C, and 81C.

CAUTION
Do not deviate from the procedures described in this section. Call processing can stop if procedural steps are not followed properly.

Determine slots and shelves

The clock controller card position varies from system to system. Table 4 shows the systems, the shelves used, and the available slot or slots.

Table 4
Clock Controller shelves and slots

System	Shelf	Slot(s)
51C, 61C	NT6D39 CPU/NET	9
81C	NTDA35 Network Module	13

Set switches

Before installing a clock controller, set the switches as shown in Table 5, Table 6, and Table 7. Table 5 displays the settings for different vintages of the QPC471. Table 6 for the QPC775, and Table 7 for the NTRB53.

Table 5
Clock Controller switch settings for QPC471 vintage H

System	SW1				SW2				SW4			
	1	2	3	4	1	2	3	4	1	2	3	4
51C, 61C	on	on	on	on	off	off	off	off	off	on	*	*
81	off	off	off	off	off	off	off	off	off	on	*	*
81C	on	off	off	off	off	off	off	off	**	on	*	*
81C with Fiber Network	on	off	off	off	off	off	off	off	**	on	*	*
					*Cable length between the J3 faceplate connectors:							
					0–4.3 m (0–14 ft)						off	off
					4.6–6.1 m (15–20 ft)						off	on
					6.4–10.1 m (21–33 ft)						on	off
					10.4–15.2 m (34–50 ft)						on	on

* If there is only one clock controller card in the system, set to OFF. If there are two clock controller cards, determine the total cable length between the J3 connectors (no single cable can exceed 25 ft.) and set these two switch positions for this cable length, as shown above. The maximum total (combined) length is 50 ft. Set the switches on both cards to the same settings.

** Set to ON for clock controller 0. Set to OFF for clock controller 1.

Note: FNF based-systems the total clock path length is equal to the length of the NTRC49 cable used to connect between the two clock controller cards.

Table 6
Clock Controller switch settings for QPC775

System	SW2	SW3	SW4
51C, 61C	ON	OFF	ON
81C	OFF	OFF	ON

Table 7
Clock Controller switch settings for NTRB53

Multigroup/ Singlegroup	Machine Type # 1	Faceplate Cable Length (CC to CC)			Side Number	Machine Type #2
1	2	3	4		5	6
MultiGroup = Off SingleGroup = On	21E = Off 51, 61, 51C, 61C, 71, 81, 81C = On	Off	Off	0-14 ft	Side 0 = On Side 1 = Off	71, 81 = Off 21E, 51, 51C, 61, 61C, 81C = On
		Off	On	15-20 ft		
		On	Off	21-33 ft		
		On	On	34-50 ft		

Note: Switches 7 and 8 are not used.

NTRB53 Clock Controller cable lengths

The dip-switches for cable length settings on the QPC471 and QPC775 have minimal impact. This is not so with the new NTRB53 clock controller. Setting the correct cable length is necessary to ensure the cleanest clock switch-over possible.

The cable length setting must be based on the type of cable connecting the clocks. For a FIJI system, the NTRC49xx cable is used. On an IGS system, the cable is a NT8D74xx and for Option 61 systems, NT8D75xx. Table 8, Table 9, and Table 10 show the settings for dip-switch 3 and 4 of the NTRB53 clock controller for each cable type.

Table 8
FIJI clock cable lengths

Cable	Cable Length	Switch 3	Switch 4
NTRC49AA	6 feet	OFF	OFF
NTRC49BA(	20 feet	OFF	ON

IGS systems support more combinations of cables. Ideally, the cables running from each clock to the intergroup module should be the same length. The combined cable length field is the determining field for dip switch settings. Add the length of the two clock to IGM cables and set the switches appropriately. See Table 9 on page 27.

Table 9
IGS clock cable lengths

Cable	Cable Length	Combined Cable Length	Switch 3	Switch 4
NT8D74AC	4 feet	8 feet	OFF	OFF
NT8D74BC	4 feet	8 feet	OFF	OFF
NT8D74AD	6 feet	12 feet	OFF	OFF
NT8D74BD	6 feet	12 feet	OFF	OFF
NT8D74AE	8 feet	16 feet	OFF	ON
NT8D74BE	8 feet	16 feet	OFF	ON
NT8D74AF	10 feet	20 feet	OFF	ON
NT8D74BF	10 feet	20 feet	OFF	ON
NT8D74AJ	16 feet	32 feet	ON	OFF
NT8D74BJ	16 feet	32 feet	ON	OFF

Option 61 settings are very simple. For an Option 61 one cable connects from the faceplate of one clock controller to the other. There are only 2 lengths available. as shown in Table 10.

Table 10
Option 61 clock cable lengths

Cable	Cable Length	Switch 3	Switch 4
NT8D75AC	4 feet	OFF	OFF
NT8D75BC(	4 feet	OFF	ON
NT8D75AC	6 feet	OFF	ON
NT8D75BD	6 feet	OFF	ON

Start the Clock Controller

The clock controller, when first enabled, is in free run mode. It stays in this mode for several minutes before being switched to tracking mode. A manual mode setting is possible using Overlay 60. All clock controllers begin tracking within approximately 15 minutes.

Clock Controller commands

During the installation procedure installers can use some of the clock controller commands in Overlay 60. Refer to *Maintenance Input/Output Guide* (553-3001-511).

See Table 11 for Overlay 39 commands with the NTRB53 clock controller.

Table 11
LD 39 commands with the NTRB53 clock controller

Command	Description	Pack/ Rel
DIS SCG x	Disable SCG card x (0 or 1). Not applicable for NTRB53 Clock Controller. Use LD 60 instead.	basic-1 basic-25.4
ENL SCG x	Enable SCG x (0 or 1). Not applicable for NTRB53 Clock Controller. Use LD 60 instead.	basic-1 basic-25.4
SCLK	Switch clock to other SCG. Functions with NTRB53 Clock Controller	basic-1 basic-25.4
STAT SCG x	Print status of SCG x (0 or 1). Prints normal status of NTRB53 (not full status)	basic-1 basic-25.4

Install or replace a Clock Controller on Option 51C, 61C half group

Use Procedure 1 to install a clock controller on a Meridian 1 Option 51C, or 61C half group.

Procedure 1
Install or replace a clock controller on a Option 51C, or 61C single group

1 Unpack and inspect circuit pack.

2 Determine the cabinet and shelf location. Refer to Table 4.

3 Set the clock controller switch. Refer to Table 5, Table 6, or Table 7.

4 Set the ENL/DIS toggle switch to DIS (disable).

5 If replacing a clock controller, perform a status check on the clock with the SSCK command in Overlay 60. The new controller should have the same status.

Note: ERR0020 messages may be generated. These can usually be ignored. However, excessive clock switching should be avoided, especially when counters are near the maintenance or out-of-service thresholds. Excessive switching could generate threshold-exceeded messages or cause the PRI to be automatically disabled. Check the counters in Overlay 60. If necessary, reset the counters using the RCNT command.

6 Set the old card's faceplate ENL/DIS switch to DIS.

7 Disconnect the cables from the old clock controller card and remove the card from the shelf.

8 If the 3PE switches have not been modified to recognize the clock controller card, adjust them.

9 Set faceplate ENL/DIS switch to DIS.

10 Install the clock controller in the selected slot.

11 Run and connect cables.

a. Connect the primary reference to J2.

b. If available, connect the secondary reference to J1.

c. Connect the cable between the two clocks to J3 on each controller card.

12 Set the faceplate ENL/DIS switch to ENL.

Note: Verify that the faceplate LED flashes three times to ensure the clock controller self test passed.

13 Enter ENL CC x in LD 60 to enable the clock controller.

14 Set the error detection thresholds and clock synchronization controls in LD 73. (Optional with card replacement; required with new installation.)

15 To track on a primary or secondary reference clock, use LD 60. Use the following command:

TRCK	PCK	(for primary)
	SCLK	(for secondary)
	FRUN	(for free-run)

16 Issue the status check command, SSCK.

Note: In order for the clock enhancement feature in the clock controller (NTRB53) to be fully functional, the user must issue a manual INI to activate the clock enhancement feature.

End of Procedure

Install or replace a Clock Controller on Option 61C/81C

Use Procedure 2 to install a clock controller on a Meridian 1 Option 61C or 81C.

Procedure 2
Install or replace a Clock Controller on Option 61C/81C

1 Unpack and inspect circuit pack.

2 Determine the cabinet and shelf location. Refer to Table 4 on page 24.

3 Set the clock controller switch. Refer to Table 5 on page 25, Table 6 on page 25, or Table 7 on page 26

4 Set the ENL/DIS toggle switch to DIS (disable).

5 If replacing a clock controller, do the following:

a. Perform a status check on the clock with the SSCK command in LD 60. The new controller should have the same status.

b. Use LD 135 to STAT the CPU and switch if necessary

c. Disable the old card using LD 60.

Note 1: Do not disable an active clock or a clock associated with an active CPU

Note 2: ERR20 messages may be generated. These can usually be ignored. However, excessive clock switching should be avoided, especially when counters are near the maintenance or out-of-service thresholds. Excessive switching could generate threshold-exceeded messages or cause the PRI to be automatically disabled. Check the counters in LD 60. If necessary, reset the counters using the RCNT command.

d. Set the old card's faceplate ENL/DIS switch to DIS.

e. Disconnect the cables from the old clock controller card and remove it from the shelf.

6 Install the new clock controller in the selected slot.

7 Run and connect the cables

a. Connect the primary reference to J2.

b. If available, connect the secondary reference to J1.

c. Connect the cable from J3 on each controller card to the junctor group connector.

8 Set the faceplate ENL/DIS switch to ENL.

9 Execute the ENL CC X command in LD 60. The faceplate LED should go to the OFF state.

10 Set the error detection thresholds and clock synchronization controls in LD 73. (Optional if replacing card; required with new installation.)

11 To track on a primary or secondary reference clock, use LD 60. The command follows:

TRCK	PCK	(for primary)
	SCLK	(for secondary)
	FRUN	(for free-run)

12 Issue the status check command, SSCK.

13 (Optional) Wait two minutes before activating the newly installed clock controller with the LD 60 SWCK command.

Note: This will allow a smooth transition of the clock controller upgrade.

14 Repeat, if necessary, for the second clock controller.

End of Procedure

Upgrade to an NTRB53 Clock Controller on Option 61C/81C

Follow these procedures to replace the existing clock controller with the NTRB53 Clock Controller on Meridian 1 large systems.

CAUTION

Clock-to-Clock cable J3 should never be connected between the old clock (QPC471 or QPC775) and the new clock (NTRB53).

Note: The NTRB53 Clock Controller cannot be combined with a QPC775 or a QPC471 card in one system.

Procedure 3
Remove old equipment

1 For dual core systems, ensure the clock controller card being removed is on the inactive core. If you need to switch cores, go to Overlay 135 and enter:

LD 135	
SCPU	Switch cores
********	Exit the overlay

2 Disable the QPC775 or QPC471 Clock Controller card. At the prompt, enter:

LD 60	Load the program
SSCK x	Get status of system clock where x = 0 or 1

If the clock is active, switch clocks. At the prompt, enter:

SWCK	Switch system clock from active to standby
SSCK x	Get status of system clock where x = 0 or 1

Ensure the other clock controller is active and in the free run mode. At the prompt, enter:

SSCK x	Get status of system clock where x = 0 or 1
TRCK FRUN	Set clock controller tracking to free run

3 Disable the clock controller card you are removing. At the prompt, enter:

DIS CC x	Disable system clock controller where x = 0 or 1

4 Set the ENL/DIS switch to DIS on the card you are removing.

Note: Disabling the clock will cause the system message FIJI0022 to be displayed.

5 Tag and disconnect the cables to the card you are removing.

6 Unhook the locking devices on the card and pull it out of the card cage.

———————————— ***End of Procedure*** ————————————

Procedure 4
Install a new NTRB53 Clock Controller on Option 61.

1 Set the ENB/DIS switch to DIS on the replacement card.

2 Set the option switches on the replacement card (NTRB53). Refer to Table 7, "Clock Controller switch settings for NTRB53," on page 26.

3 Insert the replacement card into the vacated slot and hook the locking devices.

4 Connect the reference cables (J1 and J2) to the replacement card.

Note: Do not connect J3.

5 Set the ENB/DIS switch to ENB on the replacement card.

6 Software enable the card. At the prompt, enter:

LD 60
ENL CC x Enable clock controller card, where x = 0 or 1

7 Verify that the card is active. At the prompt, enter:

SSCK x Get status of system clock where x = 0 or 1
******** Exit the overlay

8 Switch to the core with the new clock. At the prompt, enter:

LD 135
SCPU Switch CPU

Note: Wait two minutes before proceeding to the next step.

CAUTION
The following procedure to faceplate disable the active clock controller is potentially service impacting.

9 Software disable the old clock controller.

LD 60
DIS CC x Disable clock controller x

10 Faceplate disable the old clock controller and remove the clock to clock cable (J3) to force the newly installed clock controller to activate.

11 Connect the Clock-to-Clock faceplate cable to J3 of the new clock controller card in the active CPU side.

CAUTION

Noise will be experienced over local and trunk calls. System FIJI alarms will also be displayed. The noise and alarms will resolve after the new clock begins tracking to the selected reference.

12 Verify that the clock controller is active. At the prompt, enter:

LD 60	
SSCK	Get status of the new system clock, where x = 0 or 1
TRCK PCK	Track primary clock, where x = 0 or 1
RCNT	Resets all alarm counters of all digital cards
****	Exit the overlay

Note: Replacing the clock controller will generate errors on the network equipment. It is recommended that all counters be reset.

13 To replace the remaining QPC775 or QPC471 clock controller card, tag and disconnect the cables to the card you are removing.

14 Unhook the locking devices on the card and pull it out of the card cage.

15 Set the ENB/DIS switch to DIS on the replacement card.

16 Set the option switches on the replacement card (NTRB53). Refer to Table 7, “Clock Controller switch settings for NTRB53,” on page 26.

17 Insert the replacement card into the selected slot and hook the locking devices.

18 Connect the reference cables (J1 and J2) and the clock-to-clock cable (J3) to the replacement card.

19 Set the ENB/DIS switch to ENB on the replacement card.

20 Software disable and enable the card. At the prompt, enter:

LD 60	
DID CC x	Disable clock controller card, where x=0 or 1
ENL CC x	Enable clock controller card, where x=0 or 1

21 Verify that the card is active. At the prompt, enter:

SSCK x	Get status of system clock, where x=0 or 1
****	Exit the overlay

Note: Wait five minutes before proceeding to next step.

22 Activate the new card and verify that it is active. At the prompt enter:

LD60	
SWCK	Switch system clock from active to standby
SSCK x	Get status of system clock, where x = 0 or 1
TRCK PCK	Track primary clock, where x = 0 or 1
RCNT	Reset alarm counters of all digital cards
****	Exit the overlay

23 Set the clock source to the status it was in before the replacement procedure.

24 Verify clock switch-over and tracking. At the prompt, enter:

SWCK	Switch system clock from active to standby
SSCK x	Get status of system clock, where x = 0 or 1
****	Exit the overlay

End of Procedure

Meridian 1

Clock Controller Description and Installation

Information is subject to change without notice. Nortel Networks reserves the right to make changes in design or components as progress in engineering and manufacturing may warrant. This equipment has been tested and found to comply with the limits for a Class A digital device pursuant to Part 15 of the FCC rules, and the radio interference regulations of Industry Canada. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses and can radiate radio frequency energy, and if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at their own expense.
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