

297-1001-130

DMS-100 Family

Synchronous Clock System Description

Description

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NORTEL
NORTHERN TELECOM

DMS-100 Family

Synchronous Clock System Description

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Allowing this equipment to be operated in such a manner as to not provide for proper answer supervision is a violation of Part 68 of FCC Rules, Docket No. 89-114, 55FR46066

The SL-100 system is certified by the Canadian Standards Association (CSA) with the Nationally Recognized Testing Laboratory (NRTL).

This equipment is capable of providing users with access to interstate providers of operator services through the use of equal access codes. Modifications by aggregators to alter these capabilities is a violation of the Telephone Operator Consumer Service Improvement Act of 1990 and Part 68 of the FCC Rules

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Publication history

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Standard 03.03. Document migrated into new template.

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List of terms

About this document

When to use this document

This publication outlines the possible synchronous clock system configurations, lists performance objectives, gives a general description of the synchronization loop within a DMS-100 Family switch, and outlines maintenance features of the clock system.

How to check the version and issue of this document

The version and issue of the document are indicated by numbers, for example, 01.01.

The first two digits indicate the version. The version number increases each time the document is updated to support a new software release. For example, the first release of a document is 01.01. In the *next* software release cycle, the first release of the same document is 02.01.

The second two digits indicate the issue. The issue number increases each time the document is revised but rereleased in the *same* software release cycle. For example, the second release of a document in the same software release cycle is 01.02.

To determine which version of this document applies to the software in your office and how documentation for your product is organized, check the release information in *Product Documentation Directory*, 297-8991-001.

References in this document

The following documents are referred to in this document:

- *Product Documentation Directory*, 297-8991-001
- *SuperNode Technical Specification*, PLN-5001-001
- *Network Description Types NT0X48 and NT5X13*, 297-1001-102
- *Peripheral Modules*, 297-1001-103
- *Commands Reference Manual*, 297-1001-822
- *Log Reports Reference Manual*, 297-YYYY-840
- *Trunks Maintenance Guide*, 297-1001-595

- *DMS SuperNode and DMS SuperNode SE Computing Module Maintenance Guide, 297-5001-548*

What precautionary messages mean

The types of precautionary messages used in NT documents include attention boxes and danger, warning, and caution messages.

An attention box identifies information that is necessary for the proper performance of a procedure or task or the correct interpretation of information or data. Danger, warning, and caution messages indicate possible risks.

Examples of the precautionary messages follow.

ATTENTION Information needed to perform a task

ATTENTION

If the unused DS-3 ports are not deprovisioned before a DS-1/VT Mapper is installed, the DS-1 traffic will not be carried through the DS-1/VT Mapper, even though the DS-1/VT Mapper is properly provisioned.

DANGER Possibility of personal injury



DANGER

Risk of electrocution

Do not open the front panel of the inverter unless fuses F1, F2, and F3 have been removed. The inverter contains high-voltage lines. Until the fuses are removed, the high-voltage lines are active, and you risk being electrocuted.

WARNING Possibility of equipment damage



WARNING

Damage to the backplane connector pins

Align the card before seating it, to avoid bending the backplane connector pins. Use light thumb pressure to align the card with the connectors. Next, use the levers on the card to seat the card into the connectors.

CAUTION Possibility of service interruption or degradation



CAUTION

Possible loss of service

Before continuing, confirm that you are removing the card from the inactive unit of the peripheral module. Subscriber service will be lost if you remove a card from the active unit.

How commands, parameters, and responses are represented

Commands, parameters, and responses in this document conform to the following conventions.

Input prompt (>)

An input prompt (>) indicates that the information that follows is a command:

>BSY

Commands and fixed parameters

Commands and fixed parameters that are entered at a MAP terminal are shown in uppercase letters:

>BSY CTRL

Variables

Variables are shown in lowercase letters:

>BSY CTRL ctrl_no

The letters or numbers that the variable represents must be entered. Each variable is explained in a list that follows the command string.

Responses

Responses correspond to the MAP display and are shown in a different type:

```
FP 3 Busy CTRL 0: Command request has been submitted.  
FP 3 Busy CTRL 0: Command passed.
```

The following excerpt from a procedure shows the command syntax used in this document:

- 1 Manually busy the CTRL on the inactive plane by typing

>BSY CTRL ctrl_no

and pressing the Enter key.

where

ctrl_no is the number of the CTRL (0 or 1)

Example of a MAP response:

FP 3 Busy CTRL 0: Command request has been submitted.

FP 3 Busy CTRL 0: Command passed.

Introduction

This practice outlines the possible synchronous clock system configurations, lists performance objectives, gives a general description of the synchronization loop within a DMS-100 Family switch, and outlines maintenance features of the clock system.

The purpose of the synchronous clock system in a DMS-100 Family office is to provide an active Central Message Controller (CMC) clock which is inter-office synchronizable with other offices in a hierarchical timing network.

Intra-office synchronization is achieved by synchronizing the two CMC clocks in the office to each other. The active CMC clock provides timing for the Input/Output Controller (IOC), Network Modules (NM), and Peripheral Modules (PM). If the active clock becomes faulty, the inactive CMC clock is made active by the system and will continue to provide timing for the IOC, NM, and PM. Because the two CMC clocks were synchronized at the time of this transition, there will be no interruption of the timing supplied by the CMC clocks.

Inter-office synchronization is the system of keeping the active CMC clocks in two digitally connected offices in synchronization. This prevents loss of data or slips in the data transmissions between these offices.

Practice application

The information contained in this Practice is applicable to offices having Batch Change Supplement (BCS) release 14 through 19 software.

It is also applicable to offices having a BCS release greater than 19 unless reissued. The application of all Northern Telecom Practices (NTP) editions with respect to a given BCS release is given in *Product Documentation Directory*, 297-8991-001.

Reason for reissue

This document is reissued to revise the formulas of the Frequency Capture Width (FCW) and the Frequency Shift Ratio (FSR), of the clocks, as defined in Performance Objectives section.

Software identification

Software applicable to a specific DMS-100 Family office is identified by a BCS release number and by Northern Telecom (NT) Product Engineering Codes (PEC). The significance of the BCS number and the PEC is described in *Provisioning Guide*, PLN-8991-104 (section 450/32) and in the Office Feature Record D-190.

A display of the BCS number and PEC for the NT feature packages available in a specific office can be obtained by entering the command string:

>DSU;INFORM LIST;LEAVE

at a Maintenance and Administration Position (MAP).

References

References listed as prerequisites are essential for an understanding of this practice. Those listed as informative contain detailed information concerning other items mentioned in this practice, but are not essential. References are inserted at the appropriate places in the text.

Note: The documents listed may exist in more than one version. See *Product Documentation Directory*, 297-8991-001 to determine the release code of the version compatible with a specific release of software.

Prerequisite References

DOCUMENT NUMBER	TITLE
297-8991-001	<i>Product Documentation Directory</i>
PLN-5001-001	<i>SuperNode Technical Specification</i>

Informative References

DOCUMENT NUMBER	TITLE
297-1001-102	<i>Network Description Types NT0X48 and NT5X13</i>
297-1001-103	<i>Peripheral Modules</i>
297-1001-822	<i>Commands Reference Manual</i>
—continued—	

Informative References (continued)

DOCUMENT NUMBER	TITLE
297-YYYY-840	<i>Log Reports Reference Manual</i>
297-1001-595	<i>Trunks Maintenance Guide</i>
GS0X48	<i>Network Frame</i>
GS1X32	<i>Central Message Controller</i>
GS1X36	<i>CMC Peripheral Interface Card</i>
GS2X31	<i>Digital Carrier Module</i>
GS2X35	<i>DS1 Line Card</i>
GS3X14	<i>Synchronizable Master Clock Counter</i>
GS3X15	<i>Synchronizable Master Clock Oscillator</i>
—end—	

Digital network synchronization

General

The digital network is synchronized using a master and slave concept, see example in Figure 1 on page 2-3. One office, the top level in the timing network hierarchy, is designated as the Network Master office and its active clock is the Network Master Clock. Timing signals derived from the Network Master Clock are passed, via digital carrier links, to one or more Slave offices. The active clock in the Slave office synchronizes to this signal and thus runs at the same frequency as the Network Master Clock. Slave offices may act as masters-of-slaves and similarly pass timing signals to other Slave offices lower in the timing network hierarchy. Thus the entire network runs at the same frequency as the Network Master Clock.

For reliability two digital carrier links are usually used to send timing signals between synchronized offices, Link 0 and Link 1. If the one being used fails, the other is used. If both links fail, the active clock, in the office isolated from its master, uses its own internal time base and is said to be free-running. The accuracy of a free-running clock is given under SLIP RATE in chapter 3 on page 3-1.

DMS-100 synchronization

DMS-100 offices use two synchronous clocks, one associated with each CMC. One clock is designated as active and it provides timing for the NM, PM, and IOC. The other clock is designated as inactive but will be redesignated as the active if the mate clock becomes faulty.

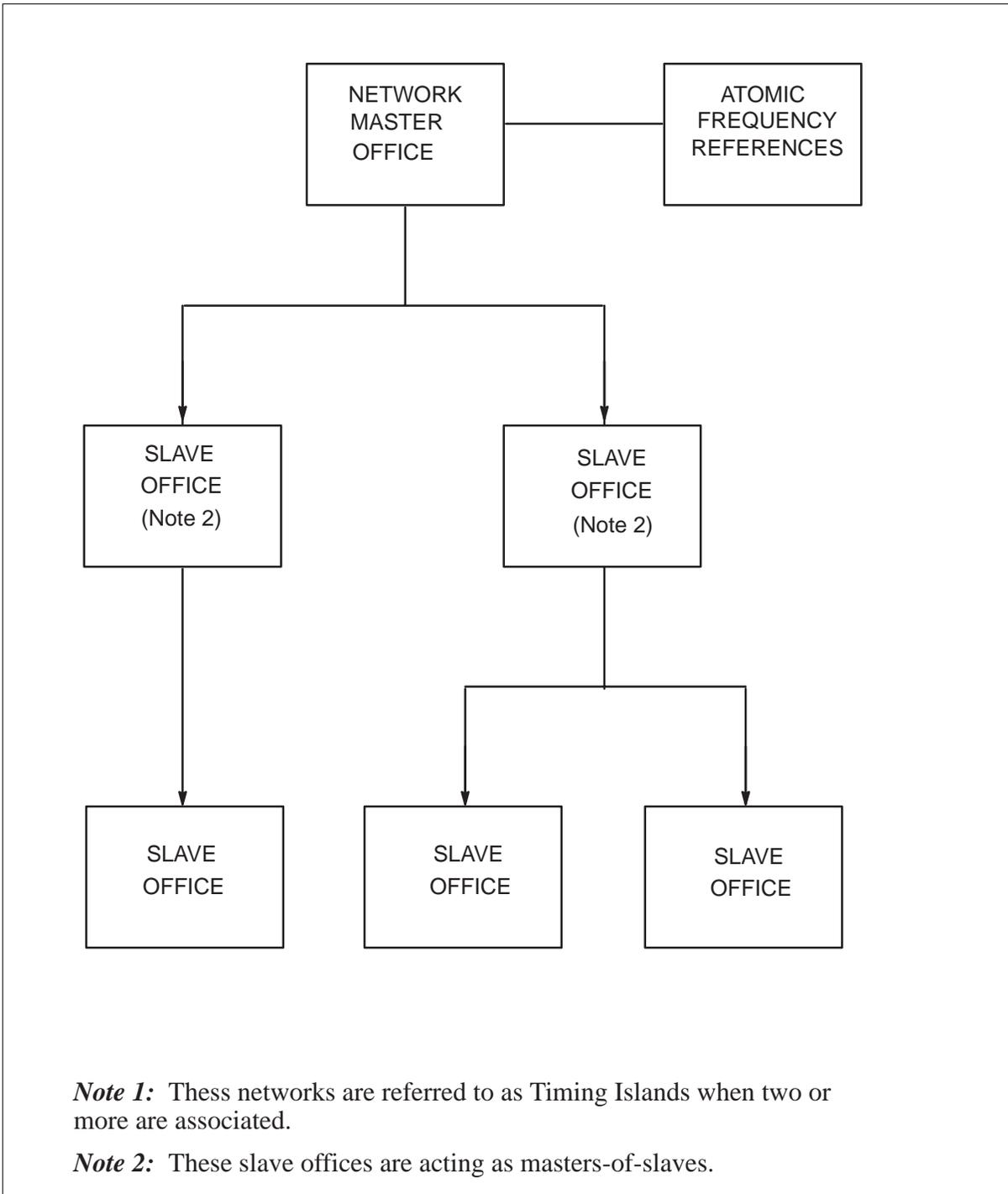
The synchronous clocks each consist of a NT3X14 clock controller card, and a NT3X15 clock card, plus a NT3x16 if the clock is a Stratum II. Together these circuit packs constitute a CMC clock capable of being synchronized to a signal external to the clock.

DMS-100 offices have two configurations of the synchronous clock system for use as Network Master office in a synchronized digital network. The Master-Internal office configuration uses its internal crystal oscillators, located on the NT3X15 or NT3X16 clock cards. The Master-External configuration uses External Reference Oscillators such as atomic clocks, for example, cesium beam oscillators.

2-2 Digital network synchronization

There is only one configuration of the synchronous clock system for use as a Slave office regardless of whether or not this slave is at the bottom of the timing network hierarchy or is acting as a master-of-slaves (see Figure 2-1 on page 2-3).

Figure 2-1
Synchronized Digital Network



2-4 Digital network synchronization

In a Master-Internal office the active clock is allowed to be free-running and the inactive clock is synchronized to the active clock (see Figure 2-2 on page 2-4). This configuration is used when an office is the master of a timing island.

In a Master-External office the active clock is synchronized to one External Reference Oscillator and the inactive clock is synchronized to another External Reference Oscillator. Neither clock is synchronized to the other, but, because of the very high accuracy of the External Reference Oscillators, the clocks are said to operate in a plesiosynchronous manner that is, very near or close to being synchronized. (see Figure 2-3 on page 2-5).

If the External Reference Oscillator associated with the active clock fails a clock activity switch will take place.

In a Slave office the active clock is synchronized to a timing signal incoming from another office. The inactive clock synchronizes to the active clock (see Figure 2-4 on page 2-6).

Both carrier links are connected to the active clock, one designated as primary, the other as alternate. Normally the active clock synchronizes to the primary link.

Figure 2-2
Master-Internal Office Configuration

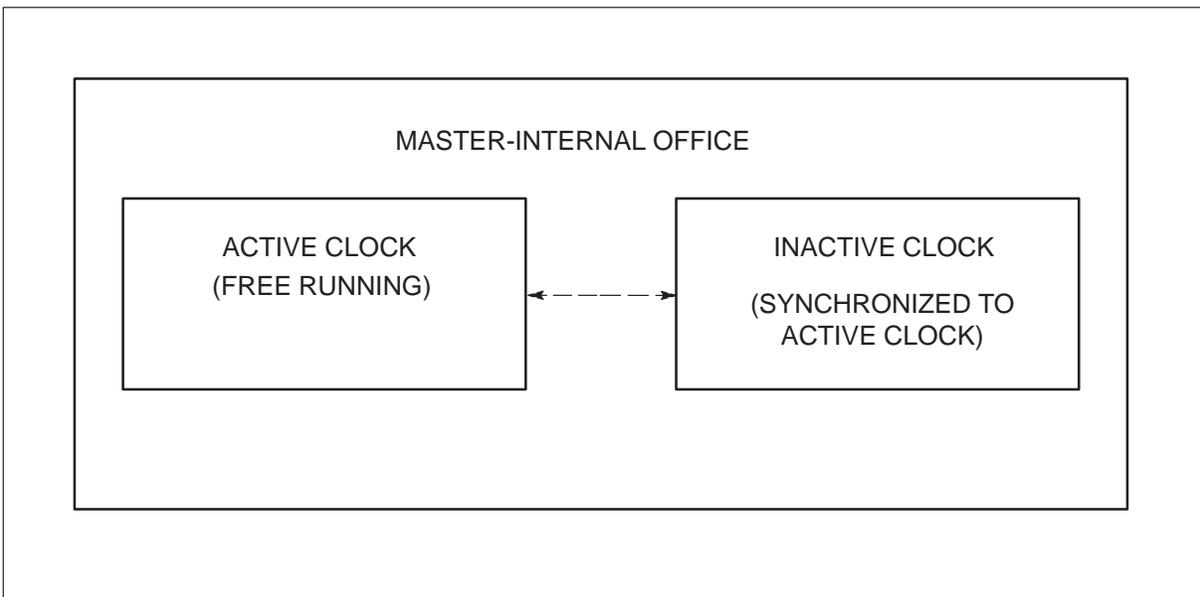


Figure 2-3
Master-External Office Configuration

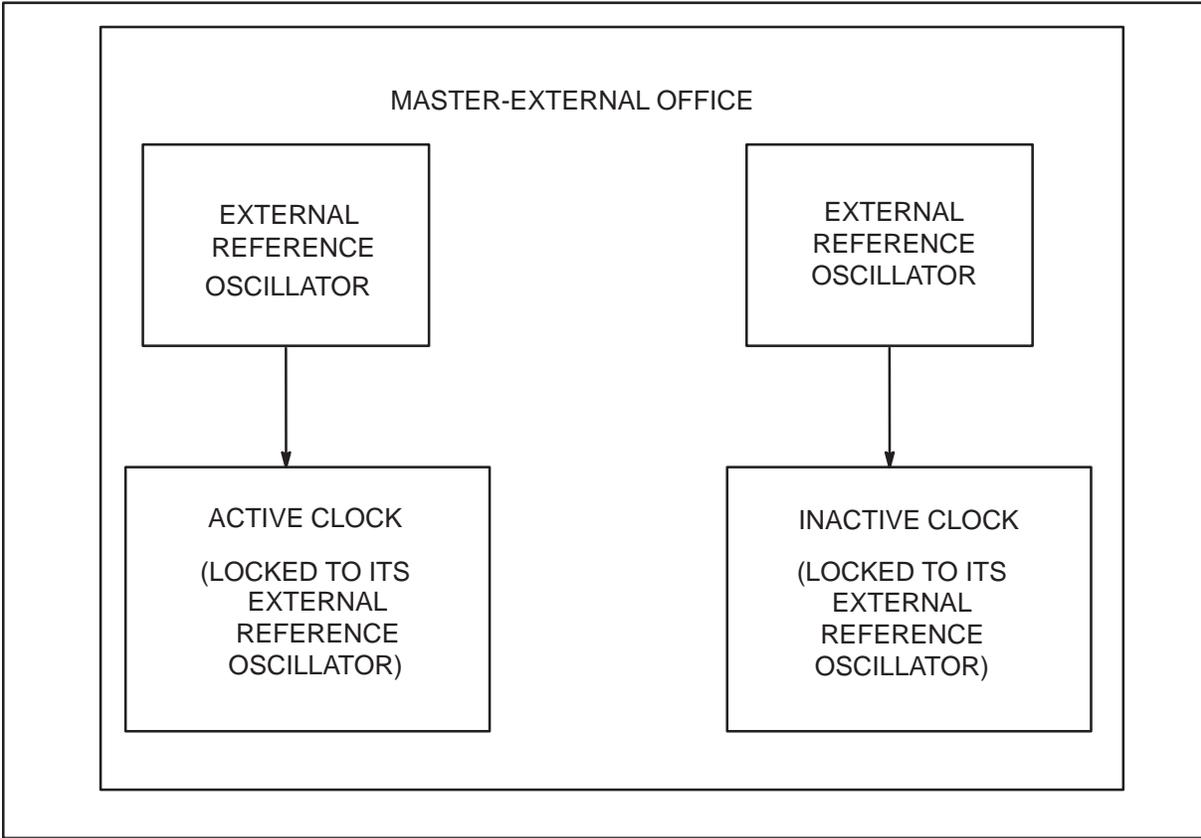
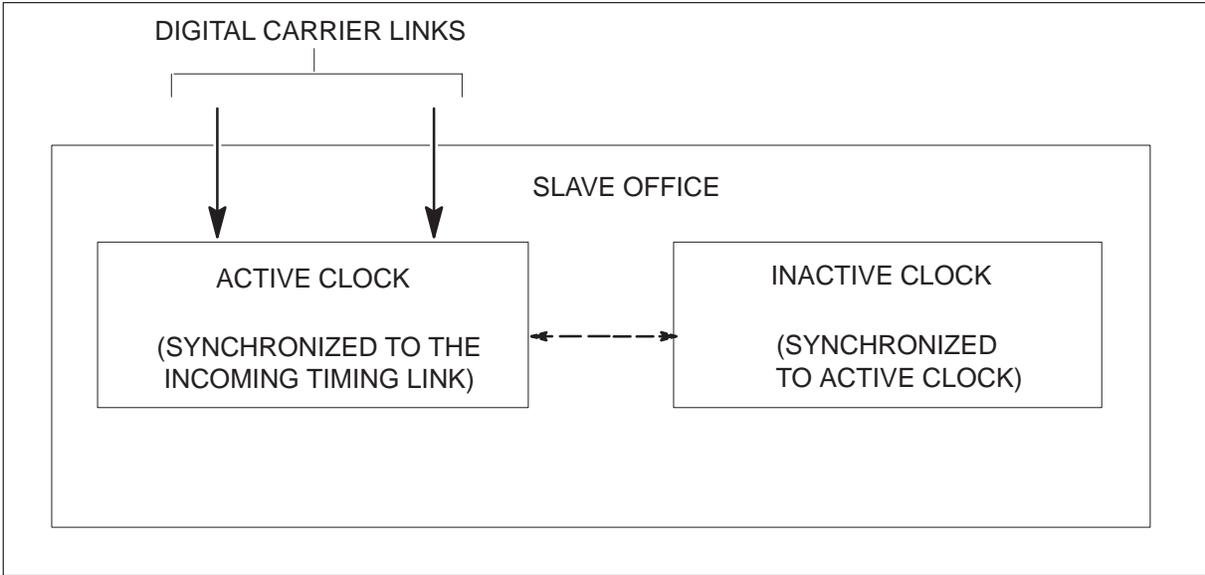


Figure 2-4
Slave Office Configuration



Performance objectives

Slip rate

When two offices are synchronized no slips should occur on digital carrier links between these two offices. Should synchronization be lost due to the failure of both carrier links used for clock synchronizing between offices, the slave enters a free-running mode. The slip rate objective while in the free-running mode is as follows:

- **Stratum II:** 1 slip in 40 hours at the end of 72 hours (3 days) of operation.
- **Non-Stratum:** 1 slip in 10 hours at the end of 72 hours of operation.
- **Stratum III:** 255 slips in 24 hours of operation, free-running.

Frequency capture width

When two offices, for example a Master and Slave, are set into synchronization there may be a frequency difference between them, especially if some maintenance action has been performed while the slave office was in the free-run mode. The frequency capture width (FCW) is as follows:

- **stratum II:** FCW is $1.6 \times 10^{>8}$, meaning the system will synchronize if the Frequency Shift Ratio (FSR) is within $13.75 \times 10^{>10}$ (see Note).
- **non-stratum:** FCW is $17.5 \times 10^{>7}$, meaning the system will synchronize if the FSR is within $13.5 \times 10^{>9}$ (see Note).
- **stratum III:** FCW is $14.6 \times 10^{>6}$ meaning the system will synchronize if the FSR is within $13.7 \times 10^{>7}$ (see Note).

Note: The FSR is determined by subtracting the desired frequency from the actual frequency and dividing the difference by the desired frequency. For example, if the desired frequency is 10.24 MHz and the actual frequency is 10 240 010 Hz, the $FSR = +9.76 \times 10^{>7}$.

Clock drift

When an office is operating without external synchronization (by design in a Master-Internal office, or when external synchronization has failed in a Master-External or a Slave office) the clock drift should be as follows:

- **Stratum II:** less than a FSR of 13.75×10^{10} over 3 days.
- **Non-Stratum:** less than a FSR of 13.5×10^9 over 3 days.
- **Stratum III:** less than a FSR of 13.7×10^7 over 3 days.

Description of synchronous clock loop

Hardware

The basic components in the DMS-100 Family Slave office synchronous clock system include the digital link interface circuit packs and the synchronous clock hardware.

The digital link interface circuit packs (CP) are mounted in a DCM, LTC, DCA, DTC, IDTC, or in a PDTC. Interface CP are NT2X35 if in a DCM or NT6X50 if in a LTC or DTC, described in 297-1001-103.

Non-Stratum and Stratum III

The synchronous clock hardware consists of a NT3X14 clock controller card and an NT3X15 clock card. These cards are mounted in the CMC shelf and the CPU shelf respectively, or in a combined CMC/IOC shelf (see *Product Documentation Directory*, 297-8991-001). Each office has two sets of clock circuit cards, one associated with each CMC to operate as active and inactive timing sources.

The NT3X15 clock card contains its own power converter circuit which requires +12V and -12V dc sources, obtained from the CMC/IOC or CPU shelf power supply, to produce regulated and unregulated voltages for the operation of its internal circuits.

Backplane wiring options on the shelf used by the NT3X15 clock card allow it, in a Master-External office, to synchronize to signals of 10.24, 10.0, 5.0, 2.56, 2.048, 1.024, or 1.0 MHz from an External Reference Oscillator.

Stratum II

The synchronous clock hardware consists of a NT3X14 clock controller card a NT3X15 clock card and a NT3X16 Oscillator and Interface card. These cards are mounted in the CMC shelf and the CPU shelf respectively, or in a combined CMC/IOC shelf (see *Product Documentation Directory*, 297-8991-001). Each office has two sets of clock circuit cards, one associated with each CMC to operate as active and inactive timing sources.

The NT3X16 card contains its own power converter circuit which requires +24V source, obtained from the CMC/IOC or CPU shelf power supply, to produce regulated and unregulated voltages for the operation of its internal circuits.

Backplane wiring options on the shelf used by the NT3X15 clock card allow it, in a Master-External office, to synchronize to signals of 10.24, 10.0, 5.0, 2.56, 2.048, 1.024, or 1.0 MHz from an External Reference Oscillator. For Stratum II NT3X16 on NT3X45 shelf, split backplane with both oscillators on same shelf with separate power supplies.

Synchronization loop

The simplified block diagram in Figure 4-1 page 4-5 illustrates a synchronous clock system associated with one CMC. The main components are identified and their locations within the DMS-100 office are given. The active CMC clock control loop and the external control loop for the active CMC clock are also shown. The operation of these loops is discussed in general terms, for additional information see references in chapter 1.

A distributed phase-lock loop is formed by the clock oscillator whose output is distributed to all hardware modules in the DMS-100 Family office; a digital phase comparator in the DS1 Interface CP; the DMS-100 internal message system; and the control algorithm in the CPU which controls the clock oscillator frequency through a digital-to-analog converter.

The incoming timing signal received over the DS1 timing link is compared in the DS1 Interface CP with the local clock signal. Firmware in the PM (DCM, DTC, LTC, DCA, PDTC, or IDTC) samples the phase differences between the two signals and reports to the synchronous clock software through the internal message system, the PM message processor, the Network Message Controller (NMC), and the CMC message processor. In addition to checking for phase differences, the DS1 Interface CP also detects and reports slips, bipolar violations, and lost synchronization.

The PM collects phase comparison samples at 400 ms intervals. After 32 samples have been collected (12.8 seconds) a phase report is sent to the CPU. The phase report contains the 32 samples and information on any slips which may have occurred.

Non-Stratum

In the CPU control algorithm, the 32 phase values are normalized and summed. The sum and the average phase values are then multiplied by two factors to form a 30-bit word. The 12 most significant digits of this word are matched to the digital-to-analog (D/A) converter in the NT3X15 clock card through the NT3X14 clock controller card.

The D/A converter supplies a dc voltage to control the frequency of the voltage-controlled crystal oscillator (VCXO) on the NT3X15 clock card.

The VCXO is temperature controlled and is tuned by applying a dc voltage, between 0 and 5V, to a control terminal. A middle frequency of 10.24 MHz is achieved with a nominal voltage of 2.5 V. Tuning is sensitive, a voltage change of 1mV gives a FSR in the order of 1×10^{-9} .

Circuits on the NT3X15 clock card monitor oscillator supply current and the status of the heater (on or off) in the temperature control oven.

The output of the NT3X15 clock card is a 10.24 MHz square wave clock signal to the mate CMC clock, and an 8 KHz square wave clock signal to the various digital circuits in the DMS-100 office.

The phase detector in the external control loop comprises two counters which allow the oscillator of the NT3X15 clock card frequency to be compared with other sources, the clock signal from the mate CMC when in the Master-Internal or Slave office configuration, or, the clock signal from an External Reference Oscillator when in the Master-External office configuration.

Stratum II

In the CPU control algorithm, the 32 phase values are normalized and summed. The sum and the average phase values are then multiplied by two factors to form a 30-bit word. The 14 most significant digits of this word are matched to the digital-to-analog (D/A) converter in the NT3X16 oscillator card through the NT3X15 and NT3X14 cards.

The D/A converter supplies a dc voltage to control the frequency of the voltage-controlled crystal oscillator (VCXO) on the NT3X16 clock card.

The VCXO is temperature controlled and is tuned by applying a dc voltage, between 0 and 5V, to a control terminal. A middle frequency of 10.24 MHz is achieved with a nominal voltage of 2.5 V. Tuning is sensitive, a voltage change of 1mV gives a FSR in the order of 1×10^{-9} .

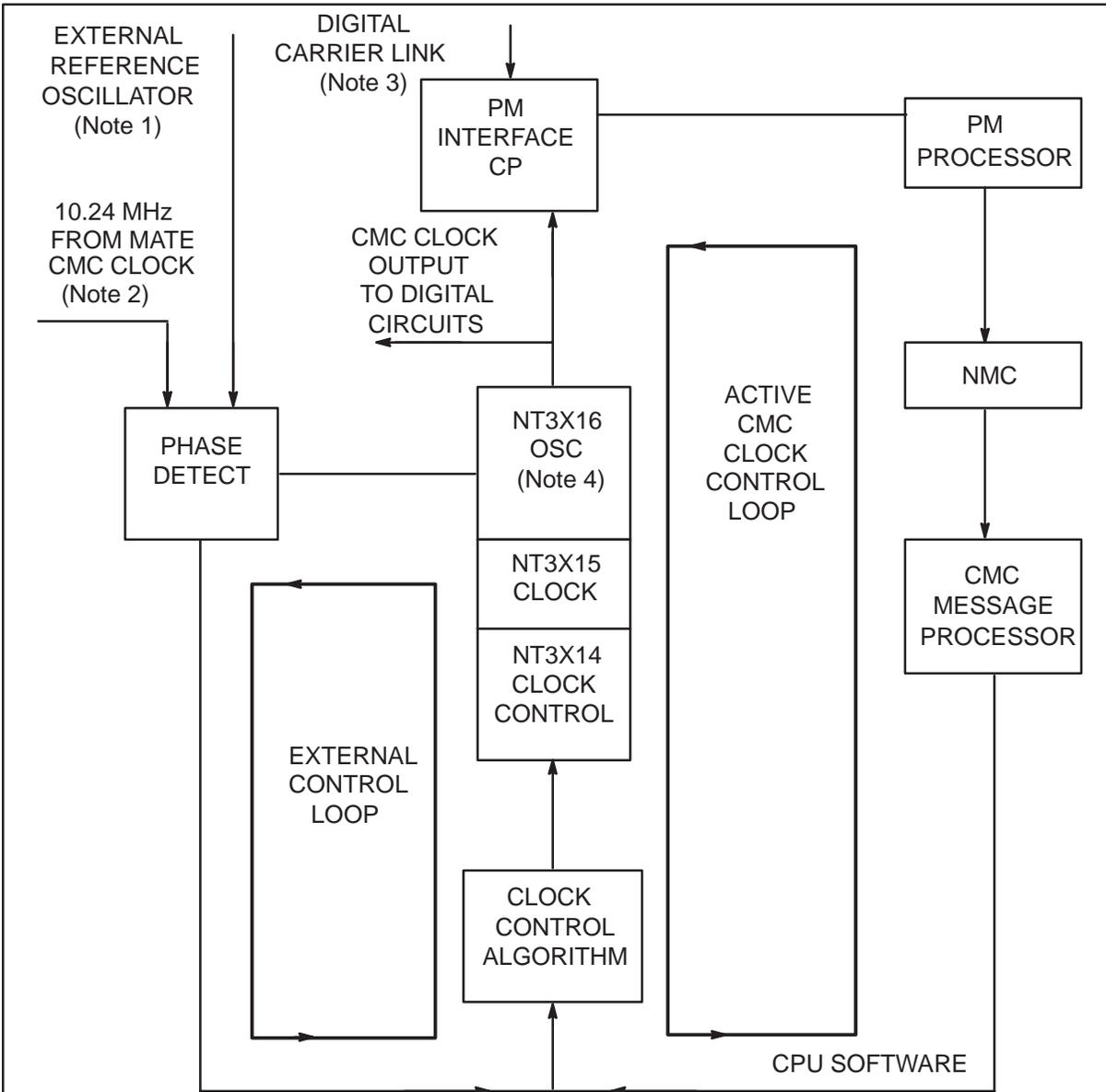
Circuits on the NT3X15 clock card monitor oscillator supply current and the status of the heater (on or off) in the temperature control oven. Heater and power alarms on 3X16 only monitor voltage converter.

The output of the NT3X16 clock card is a 10.24 MHz sine wave which is fed to the 3X15 for conversion to square wave clock signal to the mate CMC clock, and an 8 KHz square wave clock signal to the various digital circuits in the DMS-100 office.

4-4 Description of synchronous clock loop

The phase detector in the external control loop comprises two counters which allow the oscillator of the NT3X16 clock card frequency to be compared with other sources, the clock signal from the mate CMC when in the Master-Internal or Slave office configuration, or, the clock signal from an External Reference Oscillator when in the Master-External office configuration.

Figure 4-1
Synchronous Clock Loop



Note 1: Used only with a Master-External office.

Note 2: Used with a Master-Internal office or a Slave office (when inactive).

Note 3: Used only with a Slave office (when active).

Note 4: Used with Stratum II only

Synchronization algorithm

Three synchronization states are defined for the synchronous clock. The current state of the clock is indicated on the displays described in *DMS SuperNode and DMS SuperNode SE Computing Module Maintenance Guide*. The states are:

- **Free.** In this state the clock is free-running. No changes are made to the tuning control register in this state.
- **Linking (Lkng).** In this state the clock is attempting to synchronize. In a Slave office, the active clock synchronizes to another office, and the inactive clock synchronizes to, the active clock. In a Master-Internal office, the active clock is free-running and the inactive clock synchronizes to it. In a Master-External office the active and inactive clocks each lock to their own External Reference Oscillator.
- **Synchronized (Sync).** In this state the clock is synchronized to a timing source. See description of Linking (Lkng) state above.

When in the Lkng state, the phase-lock loop parameters are selected to provide time constants of about 173 and 236 seconds. The clock stays in the locking state as follows:

- **Non-Stratum:** For a fixed period of 200 phase samples (about 44 minutes).
- **Stratum II:** For a fixed period of 300 phase samples (about 64 minutes).

If the phase error is small enough after these samples, an additional 50 phase samples (about 11 minutes) are taken, during which the same phase error limits must be met, before the clock enters the Sync state. If the required phase limits are not met at the end of the first phase samples, or the limits are exceeded during the last 50 samples, the clock returns to the Free state.

A switch from Lkng to Sync state occurs through a change in the parameters of the synchronization algorithm. When in Sync state with a phase error near zero, a FSR of approximately 2×10^{-8} at the master can be tolerated without a slip occurring.

When in the Sync state (the clocks tracking) the phase-lock loop parameters are selected to provide time constants of approximately 0.9 hours and 2.39 days; that is, with an input frequency step the phase error will rise with a time constant of 0.9 hours and slowly decay to zero with a time constant of 2.39 days.

Maintenance

Interface

The maintenance interface for the Synchronous Clock system is the DMS-100 Maintenance and Administration Position (MAP) described in *Commands Reference Manual*. Maintenance information is displayed on a Visual Display Unit (VDU).

Three VDU displays are available to show the status of the Synchronous Clock system, and to allow the performance of maintenance checks and adjustments. Only one display is available to a specific office depending on the configuration used; that is, Master-Internal office, Master-External office, or Slave office. The applicable display is entered from the CMC status and menu display. These displays are described in *DMS SuperNode and DMS SuperNode SE Computing Module Maintenance Guide*.

Procedures

Automatic restoration of service is effected for single failures of the Synchronous Clock system, but restoration after total outages, multiple failures, and certain faults at the network is carried out using manual maintenance procedures, as described in *Product Documentation Directory*.

Manual frequency adjustment

The frequency of a free-running clock can be manually adjusted up or down at the Maintenance and Administrative Position (MAP) (See *DMS SuperNode and DMS SuperNode SE Computing Module Maintenance Guide*)

Stratum II clocks also require periodic adjustment, to re-center the oscillator frequency, to be done on a yearly basis, by Northern Telecom personnel.

Maintenance modes

The clock maintenance modes are:

- **In-Service.** This mode corresponds to a synchronization state of either Lkng or Sync.

- **System Busy.** This mode is entered when the clock is set to the synchronization state of Free due to some system maintenance action, or if a CMC is busied out. When the problem is cleared, the clock is resynchronized by the system.

On system reload restarts:

- 1 The active clock is set AFREE and runs at its frequency of operation before the restart until a manual request to synchronize is made.
- 2 The inactive clock is set IFREE and a 3-minute audit requests synchronization, if no fault is detected.

On warm or cold restarts, the clock system state is not changed.

Alarms

Normally, whenever a synchronous clock is free-running (synchronization state of Free) a fault condition is indicated and a major alarm is generated at the CMC level of the DMS-100 maintenance interface. However, the active clock of a Master-Internal clock system is always free-running and no alarm is generated because this is its correct mode of operation.

A number of fault conditions cause alarm indications to be set in the synchronous clock hardware. These indications are scanned approximately every 13 seconds, and if a fault condition is present a fault code appears on the Synchronous Clock (SynClk) display of the DMS-100 maintenance interface, and a log output report is generated. In general, when an alarm condition occurs, the display persists until a clock test is run and the test passes, at which time the alarm display is removed.

The alarms generated in all Synchronous Clock Systems are:

- **Heater (Htr).** Each clock oscillator heater should cycle at approximately 10 to 20 second intervals depending on the ambient temperature. If the heater does not cycle for approximately 5 minutes a heater alarm is displayed, a log output report is generated and, if the clock is active and the inactive clock is synchronized with no fault assigned, a clock activity switch is performed. Whether an activity switch takes place or not, the clock is left in its original synchronization state of Free, Lkng, or Sync (see SYNCHRONIZATION ALGORITHM in chapter 4). On initial power-up of a cold oscillator, the heater may remain on for several minutes. In this condition if the clock is in state IFLT, a Htr alarm is not set, but a log output report, indicating the heater alarm condition, is generated approximately every 5 minutes until the heater begins cycling.

Note 1: For synchronous clock versions using the Stratum II oscillator the heater must stay on at all times. If the status changes to OFF a heater alarm is generated.

Note 2: For synchronous clock versions using the Stratum III the heater alarm is not used.

- **Power (Pwr).** If a failure of the +15V and +24V converters for the clock occurs during normal operation an alarm is displayed and a log output report is generated. In many cases such a failure stops the oscillator, a clock interrupt occurs, and activity is automatically switched. In some cases, however, the oscillator does not stop, but shifts frequency. If the alarm is set in the active clock, an activity switch is performed as long as the inactive clock does not also have its alarm set. An alarm bit is set to indicate that a failure has occurred recently in the clock system. If this bit is set during normal operation, an alarm is displayed and a log output report is generated.
- **Phase (Phse).** The least significant bit of the phase data toggles with each phase sample at an 8 kHz rate. A consistent failure of this bit-toggling indicates a malfunction of the phase detector circuitry. If this bit does not toggle for 5 minutes a Phase alarm is set and a log output report is generated. If the Phse alarm occurs in the active clock, and the inactive clock is not in an alarm state, then a clock activity switch is performed and the active clock is set to the free-running state. If the Phse alarm occurs in the inactive clock then the inactive clock is set to the free-running state.
- **Tuning (Tun).** To detect long-term aging, the tuning control register value of each clock is checked when the clock is in the Sync state. If the tuning control value is greater than 175 percent from its midpoint value, a Tuning (Tun) alarm is set and a log output report is generated.

In a Master-External office the following additional alarms are generated:

- **External (Ext).** If the External Reference Oscillator is not set (synchronization state of active clock is Free), or if the External Reference Oscillator signal fails, an External alarm is set and a log output report is generated. If the alarm occurs for the active clock and the inactive clock is synchronized to its External Reference Oscillator, an activity switch is carried out. The clock with the alarm is set to the synchronization state of Free.
- **Alarm 0 (Alm0).** A failure of an External Reference Oscillator causes this alarm to be set; an Alarm 0 indication is displayed and a log output report is generated. If the alarm occurs for the active clock an activity switch is attempted, provided the inactive clock is synchronized to its External Reference Oscillator. The clock with the alarm is set to the Free state. This alarm is provided by the external source and may therefore be disabled.

- **Alarm 1 (Alm1).** A failure of the power supply to an External Reference Oscillator causes this alarm to be set, an Alarm 1 indication is displayed, and a log output report is generated. If the alarm occurs for the active clock, an activity switch is attempted, provided the inactive clock is synchronized to its External Reference Oscillator. The clock with the alarm is set to the Free state. This alarm is provided by the external source and may therefore be disabled.
- **Beat.** A beat frequency detector bit is toggled at the beat frequency between the two External Reference Oscillators. When the oscillators are within a tolerance of less than a FSR of 1×10^{11} , the beat frequency has a period of more than 2.7 hours. If the period is less than 2.7 hours a possible failure in an External Reference Oscillator is indicated, a Beat alarm is set and a log output report is generated, but no clock state change occurs. If the beat frequency period is satisfactory a status log output report is generated.

Timing links

Information applicable to the condition of the DS1 links used as timing links supplying clock signals is shown on the Synchronous Clock (SynClk) MAP display described in *DMS SuperNode and DMS SuperNode SE Computing Module Maintenance Guide*. Conditions under which changes in the display occur and other information applicable to maintenance are explained in the following paragraphs.

Two timing links are assigned in a Slave office, Link 0 and Link 1. If both timing links are functioning, Link 0 is selected for synchronization when the active clock is requested to synchronize.

Unless a timing link is not functioning, the two timing links should always be sending phase samples to the Synchronous Clock software, even if the clocks are in the Free state. Samples from each timing link are expected every 12.8 seconds. If no samples are received and no apparent timing link problem exists, the synchronous clock software informs the PM of the failure to receive samples. If samples are still not received the clock is set to the Free state, the timing link information for Carrier Link 0 and Link 1 (on the SynClk MAP display) is updated, and a log output report is generated.

If a timing link is busied due to maintenance action, the status indication on the MAP display is changed. If the clock was synchronized to the link which was busied, the other link is used for synchronization. If there is no link available the active clock is set to the Free state and log output reports are generated to indicate the clock and timing link states. The clock must be returned to service manually.

While the active clock is in the Sync state a relative phase shift between the two timing links is calculated. This relative phase shift value is used to

prevent a phase jump and possible slips when timing links are switched. If this condition occurs, a log output report is generated.

The Synchronous Clock (SynClk) MAP display includes a count of the number of slips which have occurred. If a slip is indicated in the phase sample message received from a timing link, a log message is generated and the slip count for the applicable link is incremented on the display. The actual group of phase samples in the sample message is also checked for validity. If a slip occurs or the sample validity check fails, a special action can occur:

- 1 If the active clock is in the Lkng state, the phase samples from the message are ignored.
- 2 If the active clock is in the Sync state when a slip occurs, the phase samples from the message are not used for clock correction. If two successive sample messages are received with slips or suspect samples, a switch of timing links is carried out.
- 3 If the active clock is in the Sync state and the phase error reaches three quarters of its maximum value, two possible actions can occur.
 - If the STANDBY timing link is in the Smp (sampling) state, a switch of timing links occurs.
 - If the STANDBY timing link is in the Idl state, the active clock is set to the Free state until manually returned to service.
- 4 If the active clock is in the Free state, no action occurs.

As phase samples are received from the timing links, a count of samples from each timing link is maintained. When abnormal counts occur, the faulty timing link is removed from service. The 3-minute audit attempts to return the timing link to service.

Log reports

Log reports are generated by the Synchronous Clock System, the format and content of each is determined by the office configuration, that is, with or without Enhanced Core.

The reports are defined as follows, for details refer to *Log Reports Reference Manual*, 297-YYYY-840:

- SYNC 101 Generated when a tuning control in a clock is updated. The tuning control change causes a clock frequency change.
- SYNC 102 Generated to give detailed status information about the clocks.
- SYNC 103 Generated by the synchronous clock system whenever a fault condition is detected.

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- SYNC 104 Generated by the Synchronous Clock (SYNC) Subsystem, whenever the system fails either an automatic or manual test.

List of terms

BCS

Batch Change Supplement

CC

Central Control

CMC

Central Message Controller

CPU

Central Processing Unit

D/A

Digital-to-Analog

DCM

Digital Carrier Module

DMS

Digital Multiplex System

DS1

Digital Transmission System, 1.544 Mb/s

DTC

Digital Trunk Controller

FSR

Frequency Shift Ratio

IDTC

International DTC

IOC

Input/Output Controller

LTC

Line Trunk Controller

MAP

Maintenance and Administration Position

NM

Network Module

NMC

Network Message Controller

PDTC

DTC for PCM30

PM

Peripheral Module

VCXO

Voltage-Controlled Crystal Oscillator

DMS-100 Family
Synchronous Clock System
Description
Description

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The SL-100 system is certified by the Canadian Standards Association (CSA) with the Nationally Recognized Testing Laboratory (NRTL).

This equipment is capable of providing users with access to interstate providers of operator services through the use of equal access codes. Modifications by aggregators to alter these capabilities is a violation of the Telephone Operator Consumer Service Improvement Act of 1990 and Part 68 of the FCC Rules

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